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A 1.2V 8 BIT SAR ANALOG TO DIGITAL CONVERTER IN 90NM CMOS

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ABSTRACT

Successive approximation register (SAR) analog to digital converters are widely utilized for low speed and low power applications. This paper shows a configuration of a 8 bit SAR ADC which uses monotonic capacitor switching strategy. This switching plan lessens the total capacitance in the DAC circuit which by implication prompts reduction in power consumption. Dynamic latch comparator with stack approach is utilized among the key building modules of SAR ADC, the use of this comparator lessens the leakage current in the circuit. The designed 8 bit SAR ADC is executed by utilizing 90nm CMOS technology and works at supply voltage of 1.2V. The planned SAR analog to digital converter consumes 93.01µW power.

Keywords: Analog to digital converter (ADC), capacitive network, digital to analog converter (DAC), Successive approximation register(SAR)

I. INTRODUCTION

In the fastest evolving electronic field, the hold which analog electronics has and continuously had , can never be changed or controlled in any kind of application right from old inconsequential deign to high end designs. Currently, compact gadgets have turned out to be increasingly famous. Low power dissipation is an important factor to be considered for these compact gadgets, since battery life is among one of the important requirement. As the interface between analog signal and digital signal, the analog to digital converter is a standout amongst the most vital blocks in the circuits. The analog to digital converter (ADC) is utilized to quantize continuous analog signal into numerical digital words.

There are different architecture of analog to digital converters among them two step and flash analog to ADC are popular solutions for small resolution and high speed application [2]. For the applications like low power and low speed, successive approximation register architecture is comprehensively used. The pipeline architecture is widely used for the applications like wireless network and digital applications like TV as these applications requires medium resolution analog to digital converters. But, the pipeline architecture demands several operational amplifiers which lead to high power dissipation.

In successive approximation register (SAR) analog to digital converter the fundamental source of power dissipation are comparator, capacitive reference DAC network digital control circuit. With the advancement of

technology the digital power consumption can be lowered, where as the power consumption of comparator and capacitive reference DAC network is confined by mismatch and noise. Without adding capacitors and switches monotonic switching technique can reduce the power consumption by 81% and the total number of capacitance in the capacitor digital to analog (DAC) converter is minimized by 50% [1].

An 8 bit successive approximation register ADC is designed by using monotonic capacitor switching technique and is implemented in 90nm CMOS technology by using cadence virtuoso tool. The remaining part of the paper is composed in sections and those are as follows. In section II briefly explains ADC design methodology. Section III explains the working of the building blocks of SAR ADC along with its output. Section IV covers the conclusion.

II. ADC DESIGN METHODOLOGY

An analog to digital converter (ADC) is an electronic integrated circuit which converts continuous analog signal to discrete digital structure. Among other ADC architecture successive approximation register are widely used for applications that require middle range sampling speed (50 ~ 100 MHz) [3]. In this paper monotonic capacitor switching technique is used to implement SAR ADC. The Fig.1 shows the block diagram of 8 bit successive approximation register ADC.

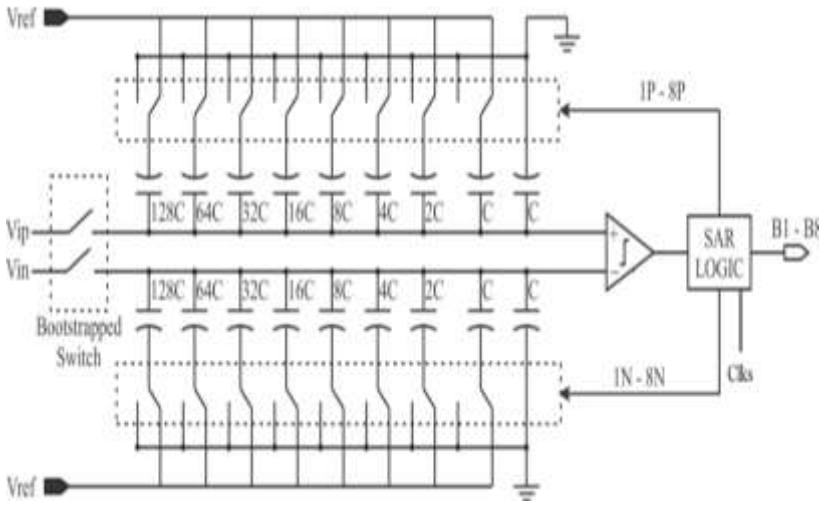

Fig.1:Block diagram of successive approximation register ADC

The Fig.1 depicts SAR ADC using monotonic capacitor switching technique. In this technique switching can occur either upward or downward. In this ADC the input signal is sampled on both top and bottom plate through the bootstrapped switches, which boosts the settling speed and input bandwidth, and at the same time the bottom plate of the capacitors are reset to V_{ref}. When the bootstrapped switch is turned off, without switching any capacitor the comparator instantly performs first comparison. Once the first comparison is done, depending on the output of the comparator the largest capacitor C_1 which is on the higher voltage potential side is switched to ground and the capacitor on the other side is remains unaltered. This process is carried out until LSB is determined. For every bit cycle, only one capacitor is switched which tends to reduce charge transfer in the capacitive DAC network and the conversion of the control circuit and switch buffer which results in lesser

power dissipation. The conventional switching technique is based on trial and error procedure, this procedure is efficient when all the attempts are successful, if the attempts are unsuccessful then it leads to more power consumption [1].

III. IMPLEMENTATION OF SAR ADC BUILDING BLOCKS

3.1 Sample and Hold circuit (S/H)

The switch in sample and hold (S/H) can be executed by utilizing basic NMOS transistor but it has a few constraints like input dependent on resistance and also input dependent charge injection. In order to enhance the performance of the switch in sample and hold the NMOS transistor can be substituted by a CMOS switch, but proper selection of aspect ratio is required in order minimize the distortion. The effective solution for this problem is utilization of bootstrap switch [4]. The below Fig.2 depicts the circuit diagram of bootstrap switch along with its output waveform. In the bootstrap switch circuit during phase S_1 the capacitor C_1 charges to $V_{DD} - V_{th}$ and during phase S_2 V_{DD} is applied to the bottom plate of the capacitor [5].

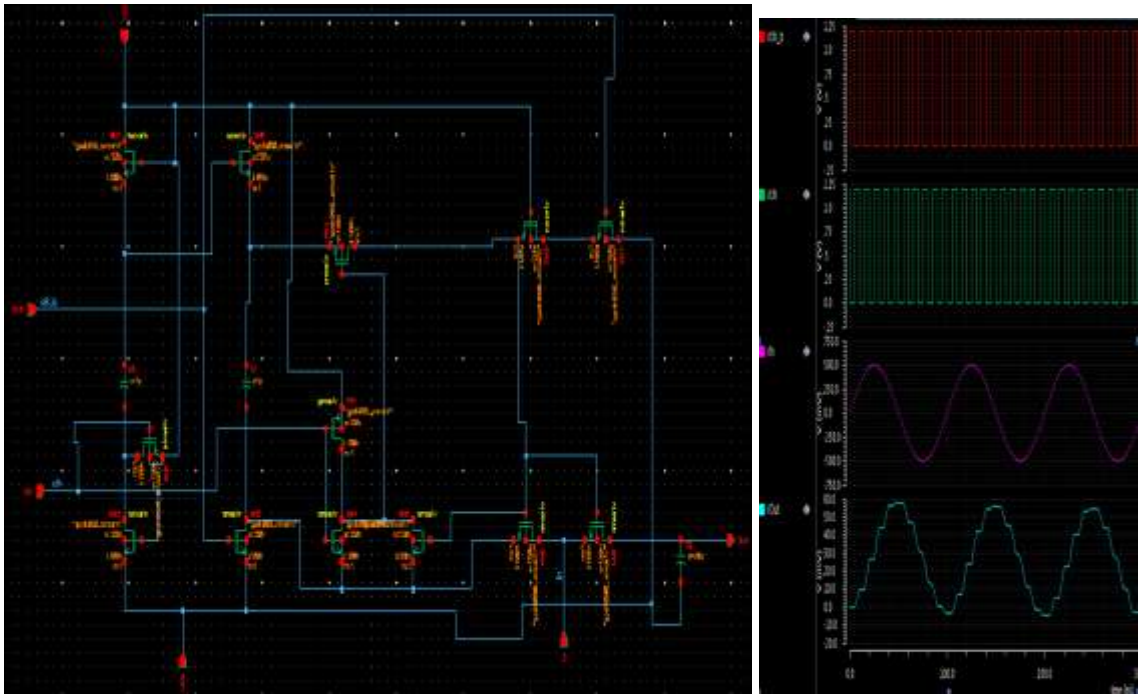

Fig.2: (a) Circuit diagram of bootstrap switch (b) Output waveform of the bootstrap switch

3.2 Dynamic latch comparator with stack approach

Comparator is an important block of successive approximation register (SAR) ADC. The comparator design has to be designed such that it consumes less power. Dynamic comparator with stack operation is used in the SAR ADC. In this technique, the components that are not in use, the voltage applied to these components is reduced by half, hence this stack approach reduces the leakage current. Fig.3 (a) and Fig.3(b) shows the schematic of the dynamic latch comparator with stack approach and its output.

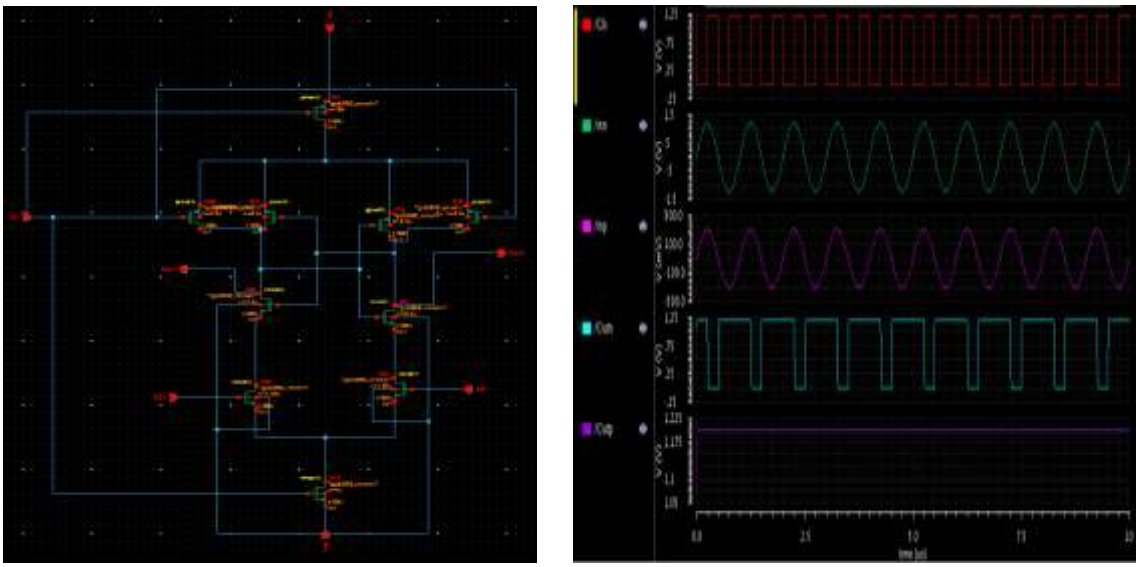

Fig.3: (a) Schematic of dynamic comparator with stack approach (b) Output of the schematic

In this circuit when the Clk = 0(low) the PMOS at the top is Mtail1 is on and the Mtail2 which the bottom NMOS is off, which leads both output node Outn and Outp to high. When Clk= 1(high) the Mtail2 is on and Mtail1 is off, the output nodes Outn and Outp which was pre charged to high voltage will starts to discharge at the rate depending on the input voltage (INN and INP)[6]. It consumes 17.15µW of power.

3.3 Digital to analog converter (DAC)

The digital to analog converter is a crucial component of SAR analog to digital converter. As depicted in Fig.1 DAC is implemented by using binary weighted capacitor array. 2N number of capacitors is present in DAC, where N is resolution or number of bits. The number of unit capacitors in capacitor array can be determined by 2^{N-1}[1]. The capacitive array DAC is implemented and DAC output is shown in Fig.4.

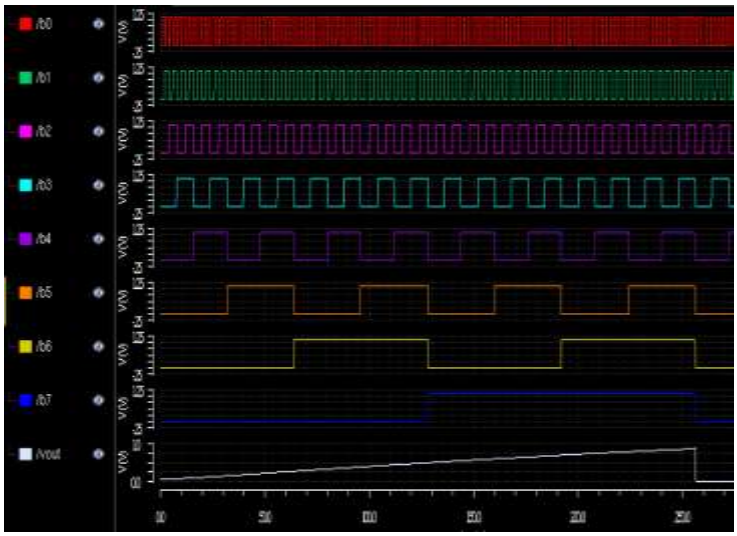

Fig.4: Digital to analog (DAC) output

3.4 SAR control logic

Asynchronous logic is chosen that clears the requirement for an additional high frequency clock to save power and enhance conversion speed. The Fig. 5 shows block diagram of asynchronous control logic. The control logic is comprised of three parts those are information register, self oscillator and shift register. The clock signal CLKC for the comparator is produced by self oscillator. OR gate is used to check the completion of the comparator and after the valid signal and the output of the OR gate is fed back to reset the comparator [7]. The output waveform of the SAR control logic is depicted in Fig. 6.

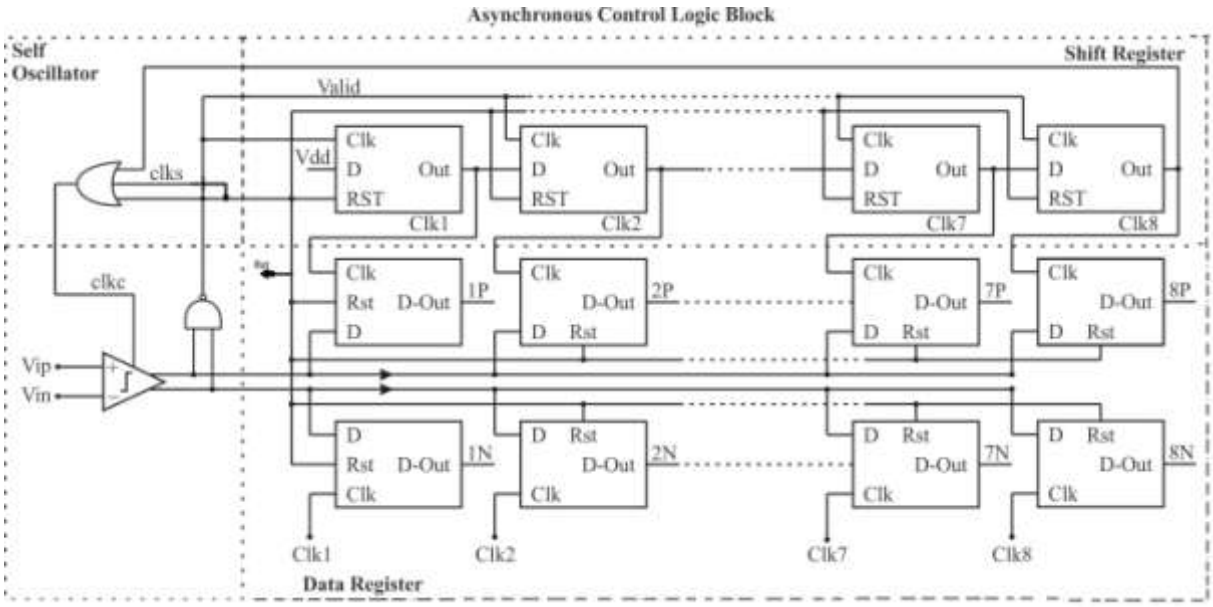

Fig.5: Block diagram of SAR control logic

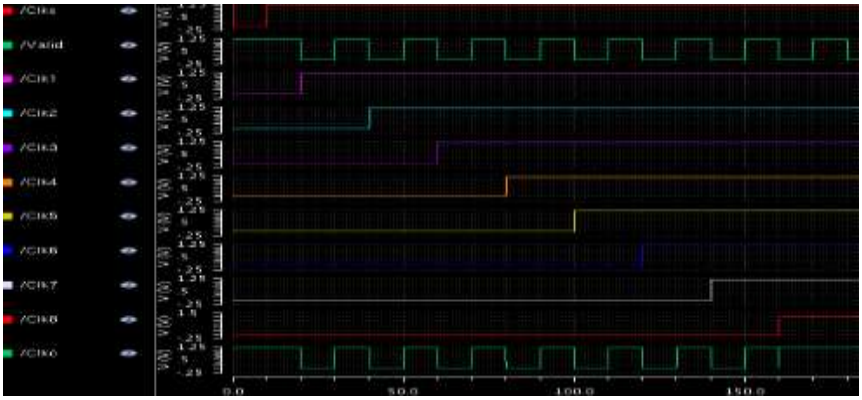

Fig.6: Output waveform of control logic

3.5 Implementation of complete SAR ADC

The key building blocks of the successive approximation register ADC are arranged in the same manner as depicted in Fig.1. The complete SAR ADC is implemented in 90nm CMOS technology by utilizing cadence virtuoso tool. The SAR ADC is verified at an applied supply voltage of 1.2V. The output of the SAR ADC is shown in below Fig. 7.

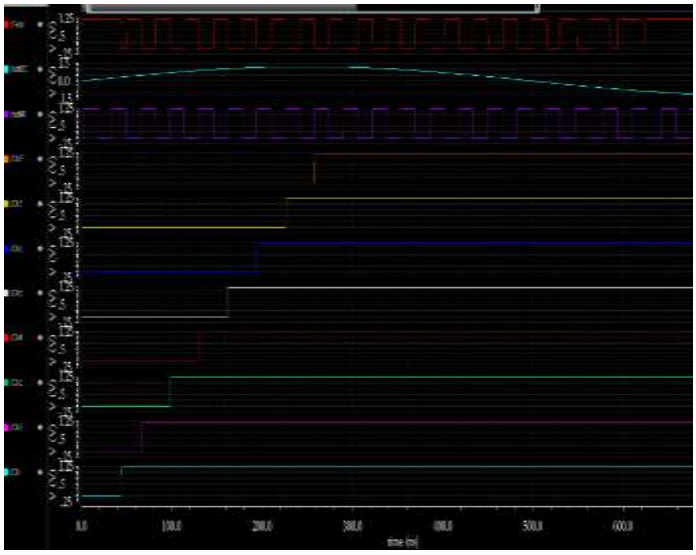

Fig.7: Output waveform of complete SAR ADC

Power analysis is carried for different voltage levels and the values obtained are given in Table I. This power analysis is compared with the work of [1] which is implemented in 90nm CMOS technology. It can be seen that at input supply voltage of 1.2 V the proposed SAR ADC using dual tail comparator consumes power of around 93.2 µW.

Table I

Power analysis comparison for different voltage levels

Supply Voltage (V)	Proposed work power consumption (P)	Power consumption of implemented paper deign [1]
1 V	37.60 µW	41.19 µW
1.2 V	93.01 µW	100 µW
1.4 V	184.68 µW	265.9 µW
1.6 V	590 µW	600.2 µW
1.8 V	1.09 mW	1.20 mW
2 V	2.36 mW	2.51 mW

IV. CONCLUSION

The designed successive approximation register (SAR) ADC is appropriate for the applications that demand the operation for low supply voltage and for medium resolution. The designed SAR ADC performance well for the applied voltage of 1.2 V and is implemented in 90nm CMOS technology. The designed SAR ADC is operated at input supply voltage of 1.2 V and consumes power around 93.2 µW. The leakage current is reduced with the usage of the stack approach dynamic latch comparator.

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