LINEARIZATION OF CASCADED BUCK CONVERTER

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ABSTRACT

The present work deals with the modeling and the stability analysis of the cascaded converters. When a converter tightly regulates its output, it behaves as a constant power load (CPL). The problem of CPLs is that they show negative incremental resistance that causes instability in the system because the control to output transfer function possessed a RHP pole. Hence the CPL has been modeled and linearized to study its effect on the source converter. The effect of the introduction of small resistance in series with inductor of source converter on the stability was analyzed. Also the compensation on the basis of the passive components i.e. Snubbers were designed so as to reduce the power dissipation due to the resistance.

Index Terms: **Buck converter, CPL, Linearization**

I. INTRODUCTION

Development of cascaded converter with new control strategies is coming up to increase the Power Processing capability and to improve the reliability of the power electronic system. Particularly, aeronautics and telecommunication appliances require large conversion ratios. These requirements can be fulfilled either with the help of isolated step down PWM dc-dc converters or non-isolated converters. However, the use of isolated step down converters results in large switching losses that may damage the switching devices. Further, use of transformer limits the switching frequency of the converter.

The characteristics of cascaded converters and the related stability problem have been presented in [1]. The dynamics of buck converter at the subsystem level with a constant power load has been reported in [2]. Further [3-4] presents the State space averaging method of the DC-DC buck converter and the control to output transfer functions has been designed in it. The buck converter model for the same has been developed in the Simulink in [5]. Mathematical calculation of input and output impedance of closed loop converter has been done in [6]. Dynamic profile of switched mode converter or the cascaded converters has been investigated in [7]. Issues in dynamic analysis and design of interconnected DC-DC power supply system reveals that the input impedance of such a system exhibits some dynamics with the frequency and it is not constant [8].

An alternative option, for realizing larger dc conversion ratios, is cascading of the converters. This scheme mainly uses multistage approach that consists of n-basic converters connected in cascade.

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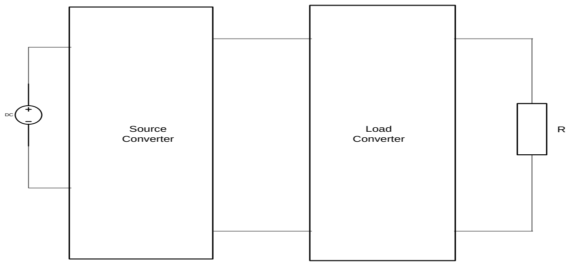

Figure 1.Cascaded Buck converter

Figure 1 shows the cascaded buck converter.

One of the converters is treated as source converter and other as load converter.

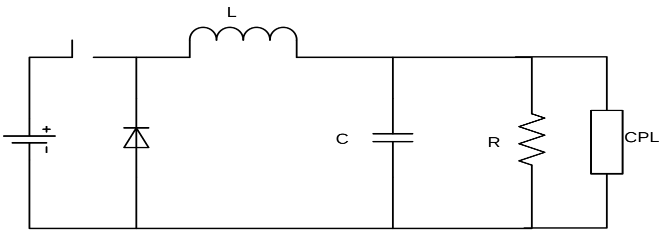

Figure 2 DC-DC Buck converter loaded by a CPL

Figure 2 shows dc-dc buck converter loaded by a constant power load. Here the load converter is treated as constant power load as the output power of the converter is constant.

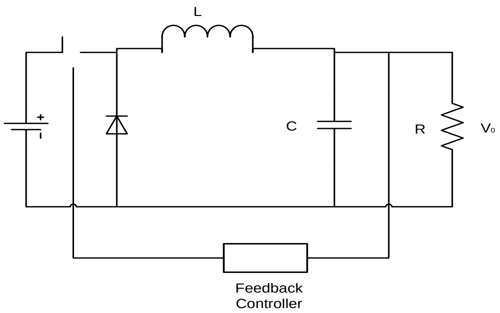

Figure 3 Tightly regulated DC-DC buck converter

Figure 3 shows a dc-dc buck converter with feedback controller. The output voltage is fed back which control the switch by generating the duty cycle to the switch with the use of some reference voltage.

II. LINEAR MODEL OF A CPL

Output power of converter is constant at $P_{out} == \frac{V_{out}^2}{R}$ (1)

If it is assumed that the efficiency does not affected by changing the input voltage i.e. input power would be constant and equal to

$$P_{in} = \frac{P_{out}}{\eta} \quad (2)$$

For CPL

$$i = \frac{P}{V} \quad (3)$$

For a given operating point $\left(I = \dfrac{P}{V} \right)$, the rate of change in current is

$$\frac{\partial i}{\partial V} = -\frac{P}{V^2} \qquad (4)$$

i.e. voltage vs current curve for CPL can be approximately a straight line that is tangent to the curve at the operating point.

The equation of this line (current) is given by

$$i = -\frac{P}{V^2} v + 2\frac{P}{V} \qquad (5)$$

i.e. at a given operating point, a CPL can be approximated by a negative resistance parallel with a constant current source as follows:

$$R_{CPL} = -\frac{V^2}{P_{CPL}} \qquad (6)$$

$$I_{CPL} = 2\frac{P}{V} \qquad (7)$$

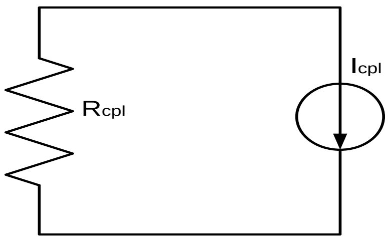

Figure 4 Equivalent representation of CPL

Figure 4 shows that constant power load can be replaced by one current source and a resistance.

Replacing equivalent circuit of CPL

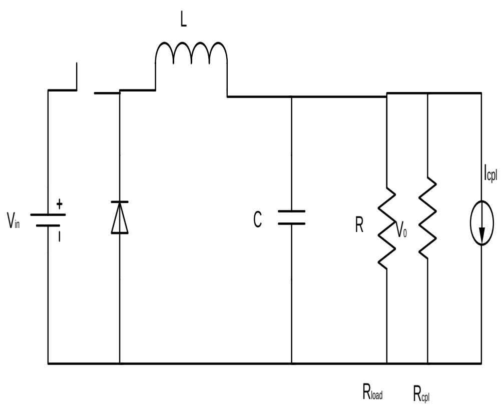

Figure 5 Buck Converter and CPL replaced with their equivalent model.

Figure 5 is the generalized model of the cascaded buck converter in which the constant power load is replaced with their respective equivalent model.

Consider a cascaded configuration in which a feeder converter is loaded by another converter that acts like a CPL. In addition, without losing the generality of the discussion, suppose that the feeder is an open-loop buck converter in CCM. To understand the effect of the CPL to the feeder system (source converter) is derived in section IV control to output transfer function, using state average method.

III. STATE SPACE DESCRIPTION OF BUCK CONVERTER

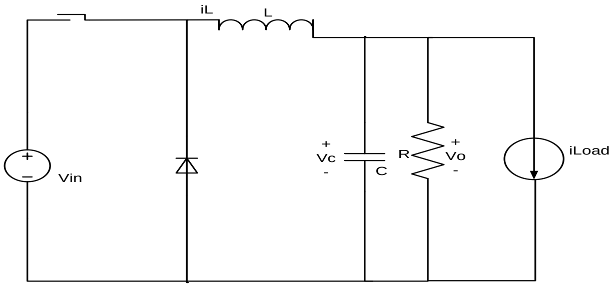

Figure 6 The circuit of the buck converter

Figure 6 shows the circuit of the cascaded buck converter in which the feeder converter is loaded by another converter that acts like a constant power load.

3.1 When Switch is in on State

When switch is ON, the equivalent circuit of the buck converter is shown in Figure 7.

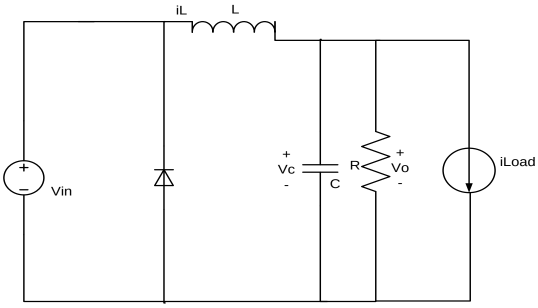

Figure 7 The buck converter when switch is in ON state.

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix} \quad (8)$$

$$v_0 = v_C \quad (9)$$

$$v_0 = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix} \quad (10)$$

State space system when switch is ON state

$$\begin{cases} \dot{x}(t) = A_1 x(t) + B_1 u(t) \\ y(t) = C_1 x(t) + E_1 u(t) \end{cases} \quad (11)$$

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}, E_1 = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{12}$$

3.2 When Switch in Off State

When switch is OFF, the equivalent circuit of the buck converter is shown in Figure 8.

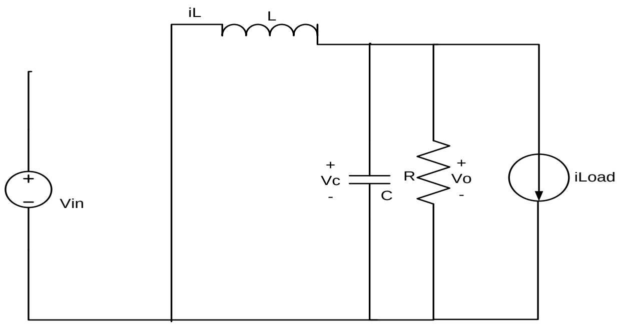

Figure 8 The buck converter when switch is in OFF state.

$$\begin{bmatrix} i_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} R_L & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix} \tag{13}$$

$$v_0 = v_C \tag{14}$$

$$v_0 = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix} \qquad 15)$$

State space system when switch is OFF State

$$\begin{cases} \dot{x}(t) = A_2 x(t) + B_2 u(t) \\ y(t) = C_2 x(t) + E_2 u(t) \end{cases} \tag{16}$$

$$A_2 = \begin{bmatrix} R_L & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, B_2 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}, E_2 = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{17}$$

IV. STATE-SPACE AVERAGE MODEL BASED TRANSFER FUNCTION

The converter behaves like switching between the two different linear time-invariant systems Equation (11) and Equation (16) during the switching period, so it looks like a time-invariant system. State-space averaging will be used in this subsection to approximate this time-variant system with a linear continuous time-invariant system. The first step is calculating a nonlinear time-invariant system by means of averaging and the second step is linearizing this nonlinear system.

The two linear systems are first averaged with respect to their duration in the switching period:

$$\begin{cases} \dfrac{dx(t)}{dt} = \left(d(t)A_1 + (1-d(t))A_2\right)x(t) + \\ \left(d(t)B_1 + (1-d(t))B_2\right)u(t) \\ y(t) = \left(d(t)C_1 + (1-d(t))C_2\right)x(t) + \\ \left(d(t)E_1 + (1-d(t))E_2\right)u(t) \end{cases} \qquad (18)$$

Equation (18) is an approximation of the time-variant system and new variable names should formally have been used. To limit the number of variable names, this is not made. The duty cycle, d(t), is an additional input signal in (4.18). A new input vector is therefore defined.

$$u'(t) = \begin{bmatrix} u(t) \\ d(t) \end{bmatrix} \qquad (19)$$

A nonlinear time-invariant system with state vector *x(t)*, input vector *u'(t)*, and output vector *y(t)*, are written as

$$\begin{cases} \dfrac{dx(t)}{dt} = f\left(x(t), u'(t)\right) \\ y(t) = g\left(x(t), u'(t)\right) \end{cases} \qquad (20)$$

Apply linearization method, where the deviations at operating point are as define:

$$\begin{cases} x(t) = X + \hat{x}(t) \\ u'(t) = U' + \hat{u}'(t) \\ y(t) = Y + \hat{y}(t) \end{cases} \qquad (21)$$

The operating-point (DC, steady state) can be denoted by the capital letters and perturbation (ac) signals can be denoted by the hat-symbol (^). Assume the operating point is at equilibrium point, i.e.

$$f\left(x(t), u'(t)\right)\Big|_{\substack{x(t)=X \\ u'(t)=U'}} = 0 \qquad (22)$$

The operating-point output values are

$$Y = g\left(x(t), u'(t)\right)\Big|_{\substack{x(t)=X \\ u'(t)=U'}} \qquad (23)$$

The following linearized (ac, small-signal) system can now be obtained from (20) (Goodwin, Graebe and Salgado, 2001, Section 3.10):

$$\begin{cases} \dfrac{d\hat{x}(t)}{dt} = A'\hat{x}(t) + B'\hat{u}'(t) \\ \hat{y}(t) = C'\hat{x}(t) + E'\hat{u}'(t) \end{cases} \qquad (24)$$

Where

$$\begin{cases} A' = \left[\dfrac{\partial f}{\partial x}\right]_{\substack{x(t)=X \\ u'(t)=U'}} \\ B' = \left[\dfrac{\partial f}{\partial u'}\right]_{\substack{x(t)=X \\ u'(t)=U'}} \\ C' = \left[\dfrac{\partial g}{\partial x}\right]_{\substack{x(t)=X \\ u'(t)=U'}} \\ D' = \left[\dfrac{\partial g}{\partial u'}\right]_{\substack{x(t)=X \\ u'(t)=U'}} \end{cases} \qquad (25)$$

Equation (24) is an approximation of the nonlinear system and new variable names should formally have been used but to limit the number of variable names, this is not made.

$$u'(t) = \begin{bmatrix} u(t) \\ d(t) \end{bmatrix} = \begin{bmatrix} U \\ D \end{bmatrix} + \begin{bmatrix} \hat{u}(t) \\ \hat{d}(t) \end{bmatrix} \quad (26)$$

$$\begin{cases} d'(t) = 1 - d(t) \\ D' = 1 - D \end{cases} \quad (27)$$

At operating point Equation (22) and Equation (23) are written using with Equation (18)

$$\begin{cases} 0 = AX + BU \\ Y = CX + EU \end{cases} \quad (28)$$

Where

$$\begin{cases} A = DA_1 + D'A_2 \\ B = DB_1 + D'B_2 \\ C = DC_1 + D'C_2 \\ E = DE_1 + D'E_2 \end{cases} \quad (29)$$

Solving eq. (28) for X and Y

$$\begin{cases} X = -A^{-1}BU \\ Y = \left(-CA^{-1}B + E\right)U \end{cases} \quad (30)$$

$$\begin{cases} A' = A \\ B' = \begin{bmatrix} \dfrac{\partial f}{\partial u} & \dfrac{\partial f}{\partial d} \end{bmatrix}_{\substack{x(t)=X \\ u'(t)=U'}} = \left[B(A_1 - A_2)X + (B_1 - B_2)U\right] = \begin{bmatrix} B & B_d \end{bmatrix} \\ C' = C \\ E' = \begin{bmatrix} \dfrac{\partial f}{\partial u} & \dfrac{\partial f}{\partial d} \end{bmatrix}_{\substack{x(t)=X \\ u'(t)=U'}} = \left[E(C_1 - C_2)X + (E_1 - E_2)U\right] = \begin{bmatrix} E & E_d \end{bmatrix} \end{cases} \quad (31)$$

Equation (24) becomes

$$\begin{cases} \dfrac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B'\hat{u}'(t) \\ \hat{y}(t) = C\hat{x}(t) + E'\hat{u}'(t) \end{cases} \quad (32)$$

Applying Laplace Transform to above equation

$$\begin{cases} s\hat{x}(s) = A\hat{x}(s) + B'\hat{u}'(s) \\ \hat{y}(s) = C\hat{x}'(s) + E'\hat{u}'(s) \end{cases} \quad (33)$$

$$\begin{cases} \hat{x}(s) = (sI - A)^{-1} B'\hat{u}'(s) \\ \hat{y}(s) = C\hat{x}'(s) + E'\hat{u}'(s) \end{cases} \quad (34)$$

V. EXTRACTING THE TRANSFER FUNCTIONS

Six transfer functions can be extracted from the above equations, but only control to output transfer function is required.

$$\begin{cases} G_{vg}(s) = \left.\dfrac{\hat{v}_0(s)}{\hat{v}_i(s)}\right|_{\hat{d}(s),\hat{g}(s)=0} = \dfrac{M(D)}{L_eCs^2 + L_eGs + 1} \\ G_{vd}(s) = \left.\dfrac{\hat{v}_0(s)}{\hat{d}(s)}\right|_{\hat{v}_i(s),\hat{g}(s)=0} = \dfrac{M(D)e(s)}{L_eCs^2 + L_eGs + 1} \\ G_{ig}(s) = \left.\dfrac{\hat{i}_L(s)}{\hat{v}_i(s)}\right|_{\hat{d}(s),\hat{g}(s)=0} = \dfrac{M(D)G\left(1+\dfrac{C}{G}s\right)}{L_eCs^2 + L_eGs + 1} \end{cases} \tag{35}$$

$$\begin{cases} G_{id}(s) = \left.\dfrac{\hat{i}_L(s)}{\hat{v}_i(s)}\right|_{\hat{v}_i(s),\hat{g}(s)=0} = \dfrac{M(D)e(s)G\left(1+\dfrac{C}{G}s\right)}{L_eCs^2 + L_eGs + 1} \\ Z_{out}(s) = \left.\dfrac{\hat{v}_0(s)}{-\hat{i}_{load}(s)}\right|_{\hat{d}(s),\hat{v}_i(s)=0} = \dfrac{L_e s}{L_eCs^2 + L_eGs + 1} \\ Z_{in}(s) = \left.\dfrac{\hat{v}_i(s)}{\hat{i}_i(s)}\right|_{\hat{d}(s),\hat{i}_{load}(s)=0} = \dfrac{1}{M(D).G_{ig}(s)} \end{cases} \tag{36}$$

Control to output transfer function

$$G_{vd} = \frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{RV_{in}}{RLCs^2 + Ls + R} \tag{37}$$

Table 1. Parameters used for Source and Load converter

PARAMETERS	SOURCE CONVERTER	LOAD CONVERTER
Frequency	100 kHz	100 kHz
Input Voltage (V_{in})	24 V	5 V
Output Voltage(V_o)	5 V	3 V
Inductor	0.87 µH	0.087 µH
Capacitor	1350 µF	1355 µF
Load Resistor	5 Ω	5 Ω
Feedback Path Transfer Function (G_c)	$G_c = \dfrac{0.04995s^2 + 1500000s + 1.5}{s}$	$G_c = \dfrac{0.04995s^2 + 1500000s + 1.5}{s}$

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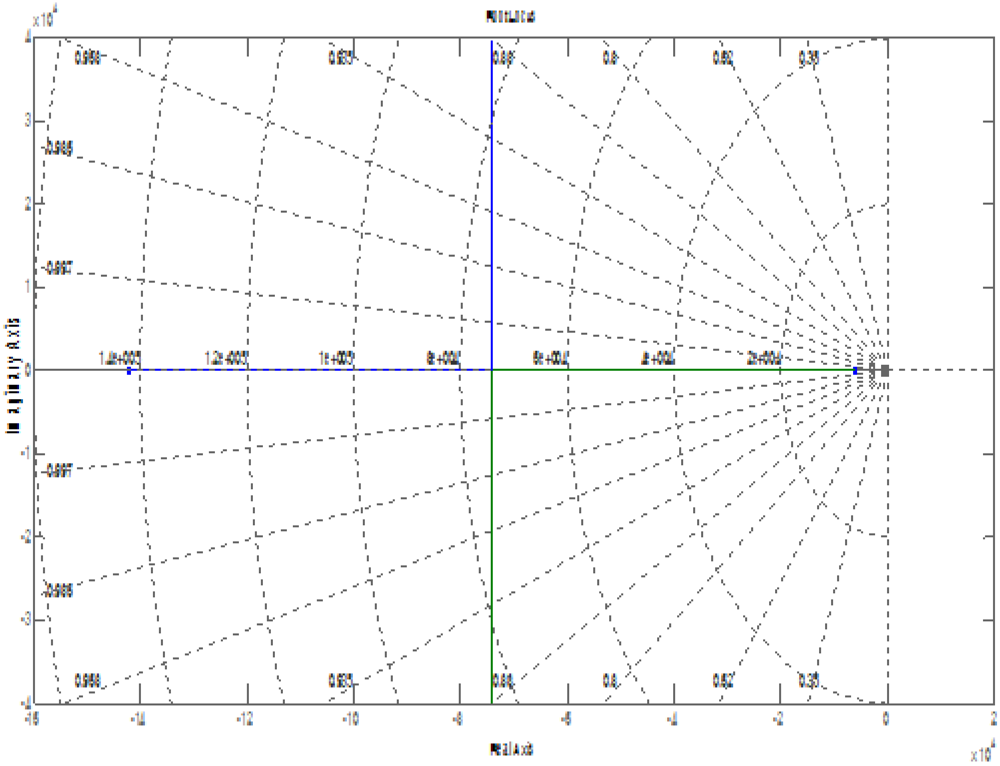

Figure 9 Root Locus Plot of control to output transfer function

VI. STABILITY ANALYSIS AND COMPENSATION

Poles of the above transfer function

Poles $$P_1, P_2 = \frac{-L \pm \sqrt{L^2 - 4R^2LC}}{2RLC} \qquad (38)$$

According to Figure 5 equivalent of R as follows

$$R = R_{Load} \| R_{CPL} \qquad (39)$$

If $R_{Load} = \infty$

$$R = R_{CPL} \qquad (40)$$

So R is negative value, Poles are in right half plane, so system will become unstable.

6.1 Compensation by R_L

By considering R_L in series with inductor, the system may become stable.

Poles of the system with R_L

$$P_1, P_2 = \frac{-(L + R_L CR) \pm \sqrt{(L + R_L CR)^2 - 4LC(R + R_L)}}{2RLC} \qquad (41)$$

If R<0 and |R|<R_L, then the system should have two real poles, and one of them should be in the right-hand side of the s-plane (right half-plane, RHP); therefore, the system should be unstable.

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If |R|>R_L and $\left(\left((L/R)+R_LC\right)^2-4LC\left(1+(R_L/R)\right)\right)<0,$

Then poles are complex conjugate, and the real value of the poles depends on the value of $\left((L/R)+R_LC\right)$.

If $\left(\left((L/R)+R_LC\right)^2-4LC\left(1+(R_L/R)\right)\right)>0,$ since $L, C, R_L > 0$ and |R|>R_L, we would have $\left|(L/R)+R_LC\right|>\left(\left((L/R)+R_LC\right)^2-4LC\left(1+(R_L/R)\right)\right)^{1/2}$. The stability of the system will depend on the value of $\left((L/R)+R_LC\right)$. In practical case |R|>R_L, so we will concentrate when |R|>R_L. From Equation (41), for making system stable $\left((L/R)+R_LC\right)$ should be positive. The value calculated from Equation (39) is negative then the stability criterion implies

$$\frac{1}{|R|}<R_LC \tag{42}$$

If Equation (42) does not hold, either R_L or C should be increased or L should be decreased to make this inequality valid.

If R_L is increased, it has to keep below |R|. Considering (39), we can stabilize the system by adding the resistance to the output of the converter but it will result more dissipation.

Let us find the amount of power dissipation that is produced by the following two cases:

1) When the compensation is done by increasing the resistive load and

2) When R_L is increased.

In the first case, a resistive load that produces a dissipation equal to P_{CPL} is required, i.e.

$$R_{Load}(Max)=\frac{V^2}{P_{CPL}} \tag{43}$$

This resistive load cancels the equivalent negative resistance of the CPL given by Equation (6). The amount of power dissipation is very large so it is not acceptable. Calculate the minimum required R_L such that the total compensation can be done by R_L i.e. $R_{Load}=\infty$. With respect to Equation (41), the minimum required R_L is

$$R_L=\frac{1}{C}\frac{1}{|R|} \tag{44}$$

$$R_{Load}=\infty \Rightarrow R=R_{CPL}=-\frac{V^2}{P_{CPL}} \tag{45}$$

Therefore

$$R_L=\frac{L}{C}\frac{P_{CPL}}{V_{out}^2} \tag{46}$$

The above value should not greater than the |R| for a stable system. With an output power equal to P_{CPL} and with output voltage V_0, the average output current, which is equal to the average inductor current, will be

$$I_L=\frac{P_{CPL}}{V} \tag{47}$$

Therefore

$$P_{R_L} = R_L I_L^2 = \frac{L}{C}\frac{P_{CPL}^3}{V^4} \qquad (48)$$

From Equation (47) we can conclude that if the output voltage is less, the power dissipation across R_L is high. In addition, as mentioned earlier, for a negative output equivalent load resistance, the necessary condition for stability is that $|R| < R_L$. Therefore, substituting

$R_L = |R| = |\infty| |R_{CPL}| = (V_{out}^2 / P_{CPL})$ and Equation (46) into Equation (47),

We have

$$P_{R_L}(Max) = \frac{V^2}{P_{CPL}}\left(\frac{P_{CPL}}{V}\right)^2 = P_{CPL} \qquad (49)$$

From Equation (49) we can say compensating the CPL by increasing R_L is more efficient than by increasing R_{Load}. Equation (49) also states that the maximum compensation that can be done with R_L will produce an amount of dissipation equal to the power of the CPL. In other words, if the amount of R_L calculated from Equation (46) produces a power dissipation more than P_{CPL}, the compensation of the CPL cannot be done only by increasing R_L.

If the ON resistance of the switch and the diode are taken into account in, the characteristic polynomial (CP) of the buck converter is calculated as follows:

$$CP = LCs^2 + \left(\frac{L}{R} + (R_s D + R_L + R_D(1-D))C\right)s + \left(\frac{R_s D + R_L + R_D(1-D)}{R} + 1\right) \qquad (50)$$

Equation (49) shows that R_s.D and R_D.(1-D) act similar to R_L and, therefore, it contributes damping to the LC system.

6.2 Compensation by Snubber Circuits

There are different circuit configuration that provides the necessary damping only near the frequencies where the LC tank can exhibit undesired oscillations. Therefore, the use of them in the circuits can reduce the power dissipation. These circuits were initially used for the damping of the input filters of the converters. However the instability problem associated with the input filter of a closed loop converter is analogous to the instability caused by the CPL loaded to a converter.

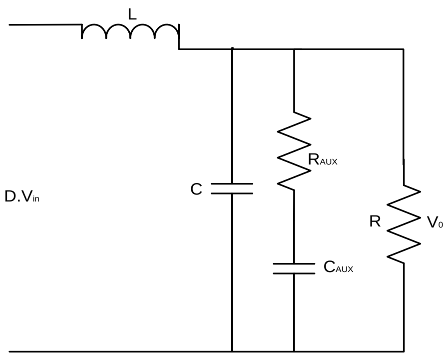

Figure 10 Buck Converter with RC Snubber

As shown in the Figure 9, an RC network has been added for providing the damping to the output of the converter. The capacitor blocks the DC current, and hence at DC level, no dissipation is produced. However, the values of R_{Aux} and C_{Aux} is selected in such a way that the capacitor acts as a short circuit while the resistance remain operating at the frequencies where the LC filter can exhibit oscillations (because of the negative resistance R).

Snubbers are small auxiliary networks the power electronics switching circuits employed for controlling the effects of circuit reactance. It aids the enhancement of circuit performance of the switching circuits and provides higher reliability, better efficiency, higher switching frequency, lesser EMI, and reduced size and weight. The basic function of a snubber in the reactive circuit is the energy absorption. This it provides necessary circuit damping, controls the rate of change of current or voltage (or it clamps the voltage overshoot).

Snubbers can be designed from either passive or active elements. Passive snubbers consist of the resistors, capacitors, inductor and diodes. Active snubbers consists of the transistors or other active switching devices, which exploits its parasitic components to serve as the function of the passive components to act as a snubber dampens the parasitic resonances in the power stage and its is mostly used among all snubber circuits. It is used for the voltage rise control for the output inductance as well as across the switches and diodes.

The capacitor and resistor values can be determined from the other circuit components. The snubber capacitance is usually two to four times the circuit capacitance value. The value of the snubber resistor can be calculated from the impedance of the parasitic resonant circuit.

Tightly regulated load converter can draw constant power from source converter shows negative resistance (-R) to source converter but load converter is having dynamics (Input Impedance).

VII. RESULTS & DISCUSSIONS

From root locus and Equation (38) it is verified that the system is unstable. Compensators are implemented to overcome this instability problem . By increasing load resistance it is observed that the power dissipation got increase. Snubber circuits are designed to reduce the power dissipation caused by increasing load resistance.

VIII.CONCLUSION

The basic DC-DC converters that operated in CCM and are loaded by CPLs have been analyzed in this chapter. Control to output transfer function is obtained and then stability analysis is done by finding the poles of the characteristic equation. The negative equivalent resistance of the CPL can be compensated by the inductor resistance.

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