THREE-PHASE FOUR-WIRE UPQC TOPOLOGY FOR POWER QUALITY IMPROVEMENT

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ABSTRACT

The current paper presents a novel control strategy of a three-phase, four-wire Unified Power Quality (UPQC) to improve power quality. The UPQC is realized by the integration of series and shunt active power filters (APF) sharing a common dc bus capacitor. The realization of shunt APF is carried out using a three-phase, four-leg Voltage Source Inverter (VSI), and the series APF is realized using a three-phase, three-leg VSI. To extract the fundamental source voltages as reference signals for series APF, a zero-crossing detector and sample-and-hold circuits are used. For the control of shunt APF, a simple scheme based on the real component of fundamental load current (I CosΦ) with reduced numbers of current sensors is applied. The average switching frequency of the switches in the VSI also reduces, consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. The proposed topology enables UPQC to compensate voltage sags, voltage swells and current harmonics with a reduced DC-link voltage without compromising its compensation capability by implementing the circuit in MATLAB/SIMULINK software.

Index Terms—Average Switching Frequency, Dc-Link Voltage, Hybrid Topology, Unified Power Quality Conditioner (UPQC).

I. INTRODUCTION

The use of sophisticated equipment/loads at transmission and distribution level has increased considerably in recent years due to the development in the semiconductor device technology. The equipment needs clean power in order to function properly. At the same time, the switching operation of these devices generates current harmonics resulting in a polluted distribution system. The power-electronics-based devices have been used to overcome the major power quality problems [1]. To provide a balance, distortion-free, and constant magnitude power to sensitive load and, at the same time, to restrict the harmonic, unbalance, and reactive power demanded by the load and hence to make the overall power distribution system more healthy, the unified power quality conditioner (UPQC) is one of the best solutions [6]. A three-phase four-wire (3P4W) distribution system can be realized by providing the neutral conductor along with the three power lines from generation station or by utilizing a delta-star (Δ–Y) transformer at distribution level. The UPQC installed for 3P4W application generally considers 3P4Wsupply . In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing . In, four-leg VSI topology for shunt active

filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, the authors proposed a T-connected transformer and three-phase VSCbased DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer.

In this paper, a UPQC topology with reduced dc-link voltage is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor.

II. CONVENTIONAL AND PROPOSED TOPOLOGIES OF UPQC

In this section, the conventional and proposed topology of the UPQC are discussed in detail. Fig. 1 shows the power circuit of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies . In this figure,vsa, vsb, and vscaresource voltages of phasesa, b, and c, respectively. Similarly, vta,vtb, andvtcare terminal voltages. The voltagesvdvra,vdvrb, and vdvrc are injected by the series active filter. The threephase source currents are represented byisa, isb, and isc, load currents are represented byila , ilb, and ilc. The shunt active filter currents are denoted byifa, ifb, ifc, and iln represents the current in the neutral leg. Ls andRs represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented byLfandRf, respectively, and the interfacing inductance and filter capacitor of the series active filter are represented byLse andCse, respectively. The load constituted of both linear and nonlinear loads as shown in this figure1. The dc-link capacitors and voltages across them are represented byCdc1=Cdc2= CdcandVdc1=Vdc2=Vdc, respectively, and the total dc-link voltage is represented byVdbus(Vdc1+Vdc2=2Vdc).Inthis conventional topology, the voltage across each common dc-link capacitor is chosen as 1.6 times the peak value of the source voltages as given in. Fig.1 represents the equivalent circuit of the proposed VSI topology for UPQC compensated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitorCf in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitorCf has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section.

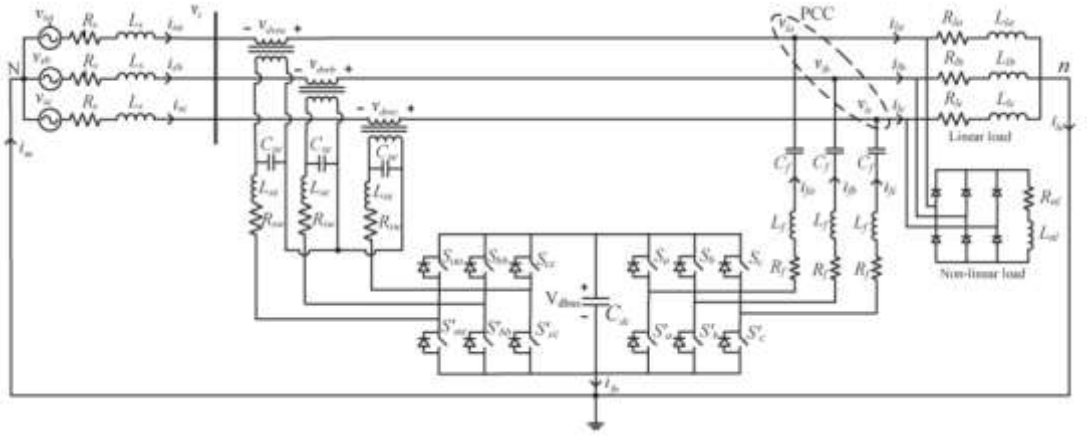

Fig. 1. Equivalent Circuit Of Proposed VSI Topology For UPQC Compensated System (Modified Topology)

The reduction in the dc-link voltage requirement of the shunt active filter enables us to the match the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitorCf and the other VSI parameters have significant effect on the performance of the compensator. These are given in the next section. This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter. Unlike the topologies mentioned in the literature this topology does not require the fourth leg in the shunt active filter for three-phase four-wire system. The performance of this topology will be explained in detailed in the following section.

III. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

In this work, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. However, the voltages still contain switching frequency components and they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation. To remove this limitation of the algorithm, fundamental positive sequence voltagesv+ la1(t), v+lb1(t), and v+lc1(t)of the PCC voltages are extracted and are used in control algorithm for shunt active filter. The expressions for reference compensator currents are given in. In this equation,Plavgis the average load power, Ploss denotes the switching losses and ohmic losses in actual compensator, and it is generated using a capacitor voltage PI controller. The termPlavgis obtained using a moving average filter of one cycle window of timeTin seconds. The termϕis the desired phase angle between the source voltage and current wherev ∗lir represents the desired load voltages in three phases, and v∗ dvri represents the reference series active filter voltages.

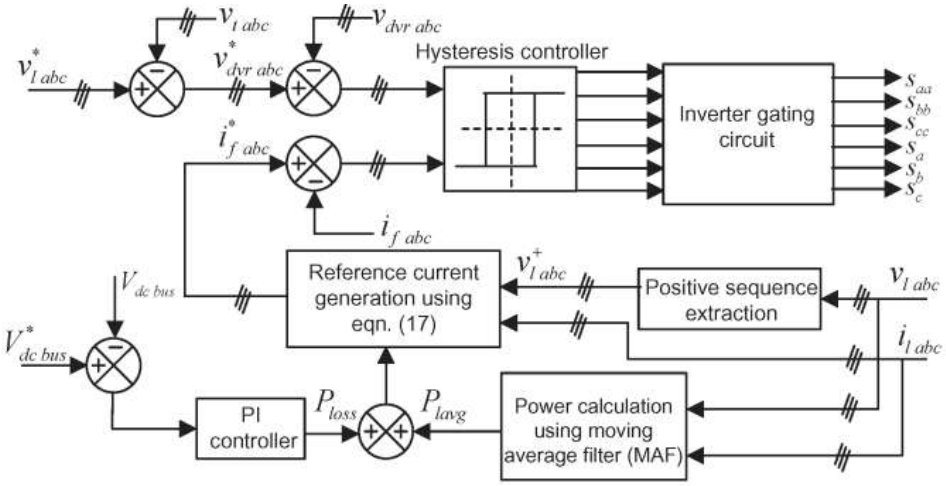

Fig. 2. Control Block Diagram For UPQC

Once the reference quantities and the actual quantities are obtained from the measurements, the switching commands for the VSI switches are generated using hysteresis band current control method. Hysteresis current controller scheme is based on a feedback loop, generally with two-level comparators. The switching commands are issued whenever the error limit exceeds a specified tolerance band "±h." Unlike the predictive controllers, the hysteresis controller has the advantage of peak current limiting capacity apart from other merits such as extremely good dynamic performance, simplicity in implementation and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it. The switching control law for shunt active filter is given as follows.

If ifa≥i∗ fa+h1, then bottom switch is turned ON whereas top switch is turned OFF(Sa=0,Sa=1).

Ififa≤i∗fa−h1, then top switch is turned ON whereas bottomswitch is turned OFF(Sa=1,Sa=0).

Similarly the switching commands for series active filter is given as follows.

If vdvra≥v∗dvra+h2, then bottom switch is turned ON whereas top switch is turned OFF(Saa=0,Saa=1).

If vdvra≤v∗ dvra−h2, then top switch is turned ON whereasbottom switch is turned OFF(Saa=1,Saa=0).

The control circuitry for both the topologies is same and is shown in Fig. 2. Only six switching commands are to be generated. These six signals along with the complementary signals will control all the 12 switches of the two inverters.

IV. SIMULATION RESULTS

In order to validate the proposed topology, simulation is carried out using graphic-driven simulation software PSCAD. The simulation results for both the conventional topology and the proposed modified topology are presented in this section for better understanding and comparison between both the topologies. The load currents and terminal (PCC) voltages before compensation are shown in Fig. 3. The load currents are unbalancedand distorted as shown in Fig. 3, the terminal voltages are also unbalanced and distorted because these load currents.

Case1: Three-Phase Four-Wire UPQC Topology.

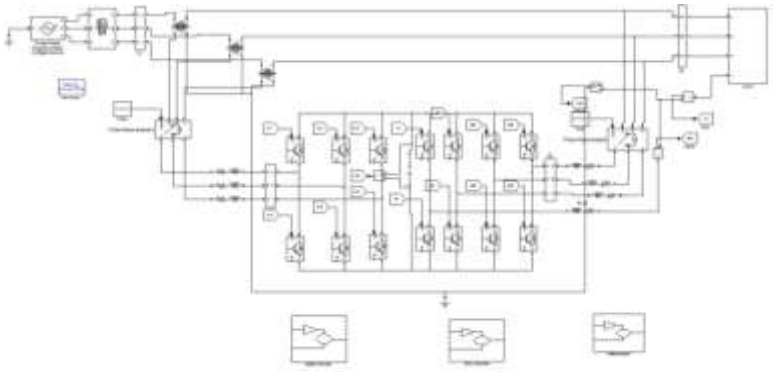

Fig. 3. MATLAB/simulink modal of Three-Phase Four-Wire UPQC Topology

Figure3 shows the MATLAB/simulink modal of Three-Phase Four-Wire UPQC Topology.

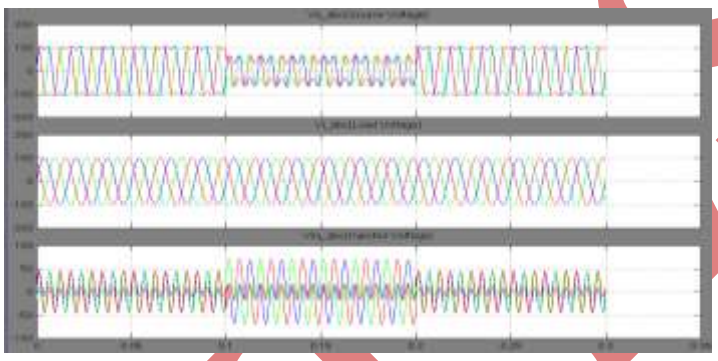

Fig. 4. Source Voltage, Load Voltage and Injected Voltage of the Three-Phase Four-Wire UPQC Topology

Figure4 shows the source voltage, load voltage and injected voltage of the Three-Phase Four-Wire UPQC Topology.

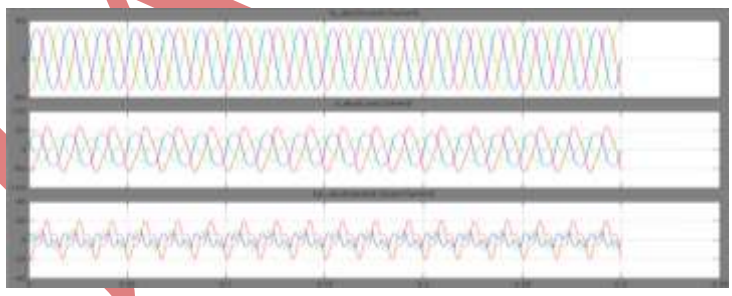

Fig. 5. Source Current, Load Current and Injected Current of the Three-Phase Four-Wire UPQC Topology

Figure5 shows the source current, load current and injected current of the Three-Phase Four-Wire UPQC Topology.

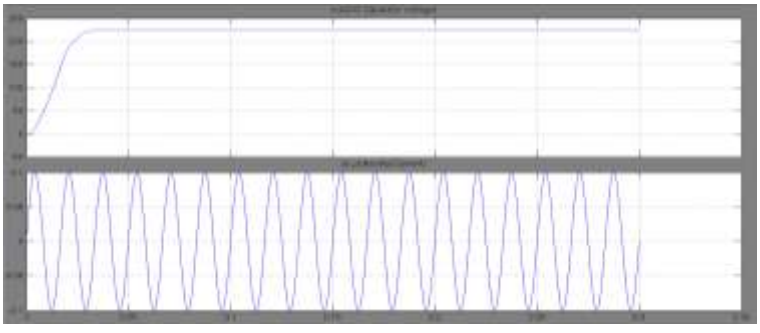

Fig. 6. Simulation Results Using Conventional Topology DC Capacitor And Neutral Current

Figure6 shows the Simulation results using conventional topology DC capacitor and neutral current.

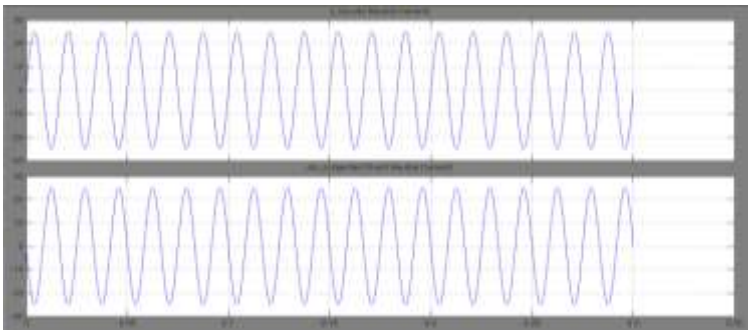

Fig. 7 Load Neutral Current and Injected Shunt Neutral Current

Figure7 shows the load neutral current and injected shunt neutral current.

Case2: Three-Phase Four-Wire UPQC Topology with arm

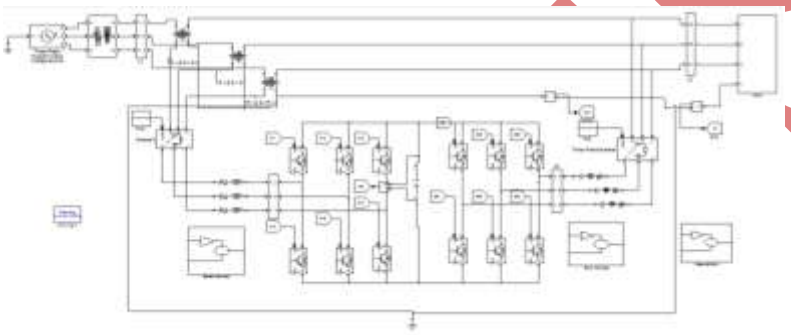

Fig. 8 MATLAB/Simulink Modal of Three-Phase Four-Wire UPQC Topology with Arm

Figure8 shows the MATLAB/simulink modal of Three-Phase Four-Wire UPQC Topology with arm.

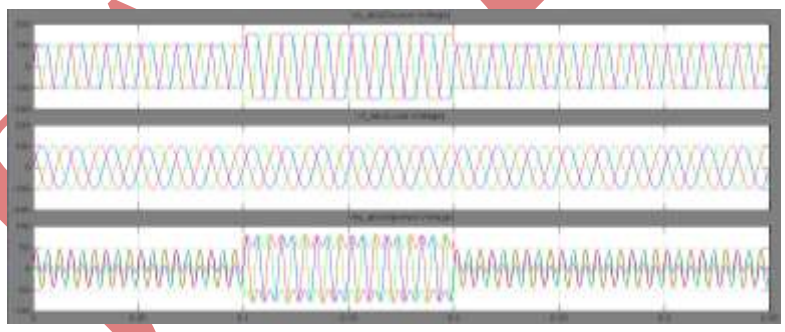

Fig. 9 Source Voltage, Load Voltage and Injected Voltage of the Three-Phase Four-Wire UPQC Topology with Arm

Figure9 shows the source voltage, load voltage and injected voltage of the Three-Phase Four-Wire UPQC Topology with arm.

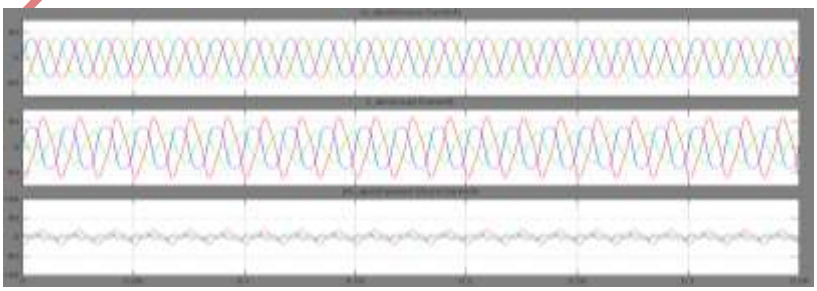

Fig. 10 Source Current, Load Current And Injected Current Of The Three-Phase Four-Wire UPQC Topology With Arm

Figure10 shows the source current, load current and injected current of the Three-Phase Four-Wire UPQC Topology with arm.

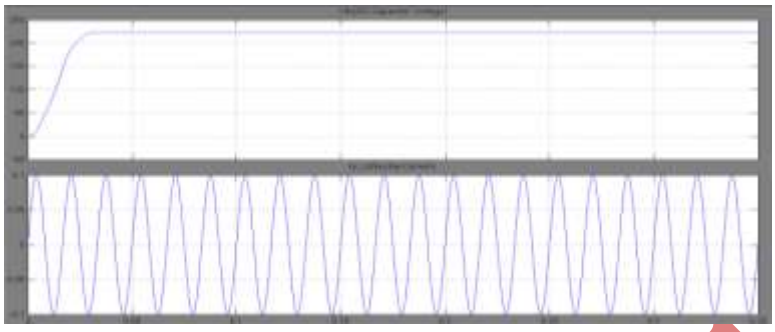

Fig. 11. Simulation Results Using Conventional Topology DC Capacitor And Neutral Current

Figure11 shows the Simulation results using conventional topology DC capacitor and neutral current.

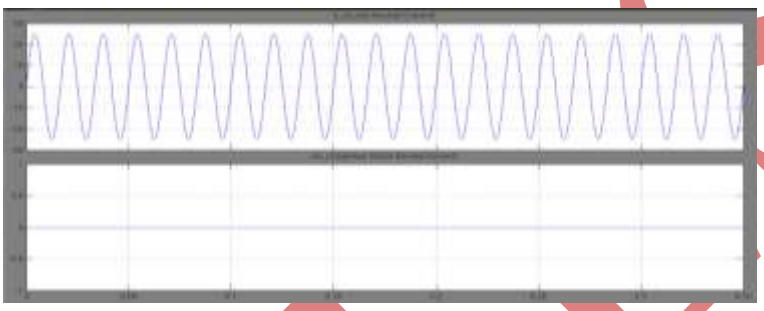

Fig. 12 Load Neutral Current And Injected Shunt Neutral Current

Figure12 shows the load neutral current and injected shunt neutral current.

Case3: Three-Phase Four-Wire UPQC Topology with sag

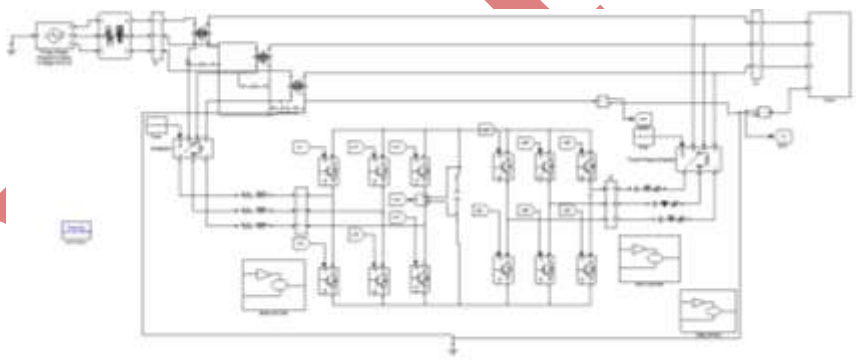

Fig. 13 MATLAB/Simulink Modal of Three-Phase Four-Wire UPQC Topology with Sag

Figure13 shows the MATLAB/simulink modal of Three-Phase Four-Wire UPQC Topology with sag

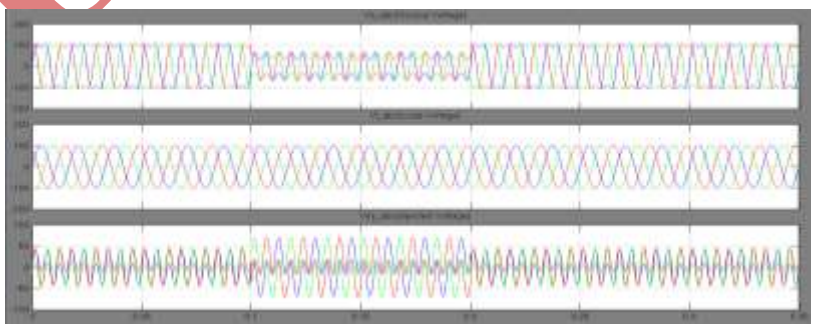

Fig. 14 Source Voltage, Load Voltage and Injected Voltage of the Three-Phase Four-Wire UPQC Topology with Sag

Figure14 shows the source voltage, load voltage and injected voltage of the Three-Phase Four-Wire UPQC Topology with sag.

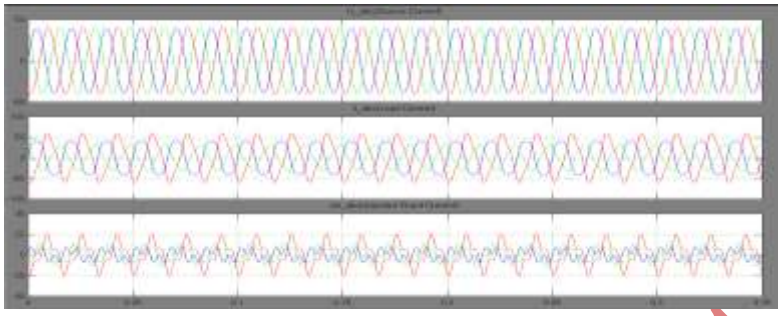

Fig. 15 Source Current, Load Current and Injected Current of the Three-Phase Four-Wire UPQC Topology with Sag

Figure15 shows the source current, load current and injected current of the Three-Phase Four-Wire UPQC Topology with sag.

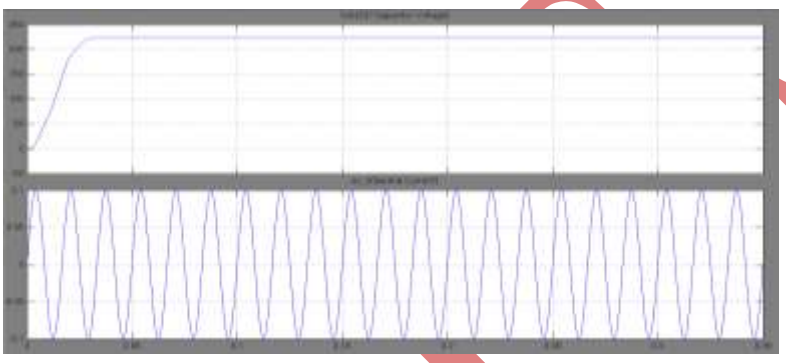

Fig. 16. Simulation Results Using Conventional Topology DC Capacitor and Neutral Current

Figure16 shows the Simulation results using conventional topology DC capacitor and neutral current.

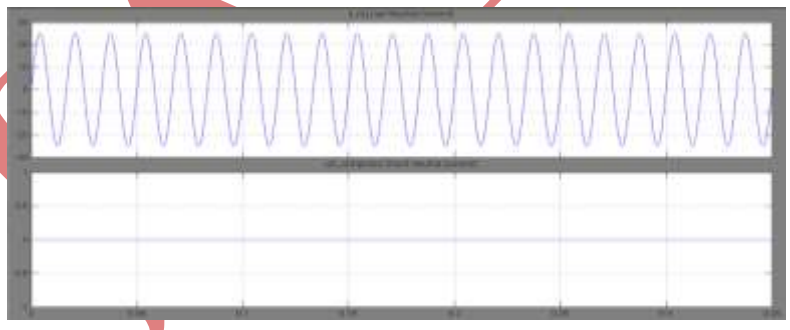

Fig. 17 Load Neutral Current and Injected Shunt Neutral Current

Figure17 shows the load neutral current and injected shunt neutral current.

Case4: Three-Phase Four-Wire UPQC Topology with sag

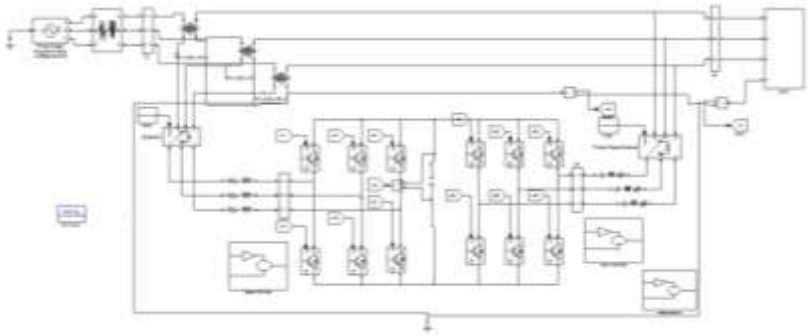

Fig. 18 MATLAB/Simulink Modal Of Three-Phase Four-Wire UPQC Topology With Swell.

Figure18 shows the MATLAB/simulink modal of Three-Phase Four-Wire UPQC Topology with swell.

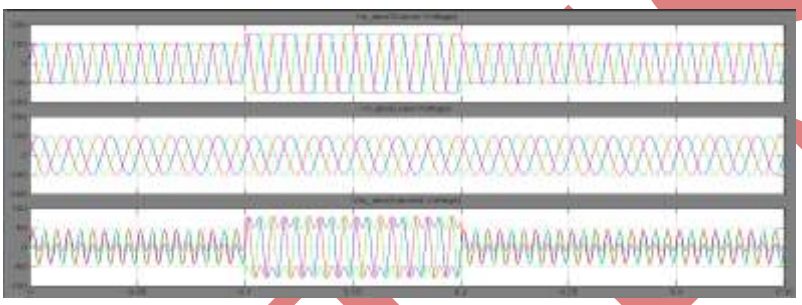

Fig. 19 Source Voltage, Load Voltage And Injected Voltage Of The Three-Phase Four-Wire UPQC Topology With Swell

Figure19 shows the source voltage, load voltage and injected voltage of the Three-Phase Four-Wire UPQC Topology with swell.

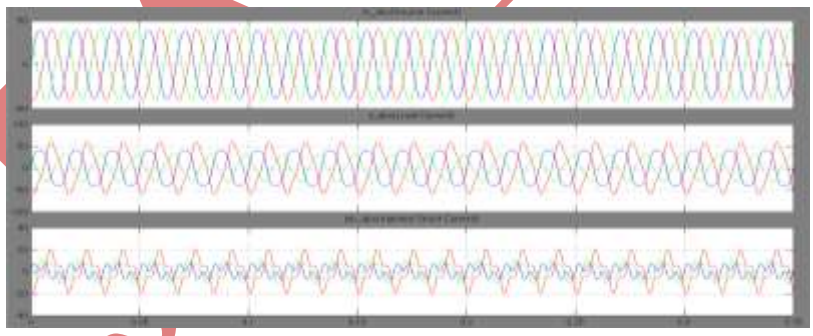

Fig. 20 Source Current, Load Current And Injected Current Of The Three-Phase Four-Wire UPQC Topology With Swell

Figure20 shows the source current, load current and injected current of the Three-Phase Four-Wire UPQC Topology with swell.

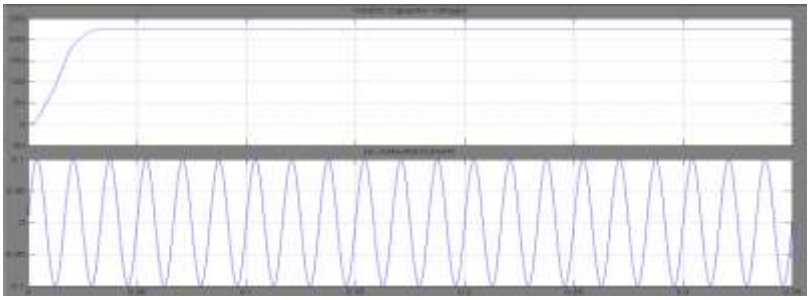

Fig. 21 Simulation Results Using Conventional Topology DC Capacitor And Neutral Current

Figure21 shows the Simulation results using conventional topology DC capacitor and neutral current.

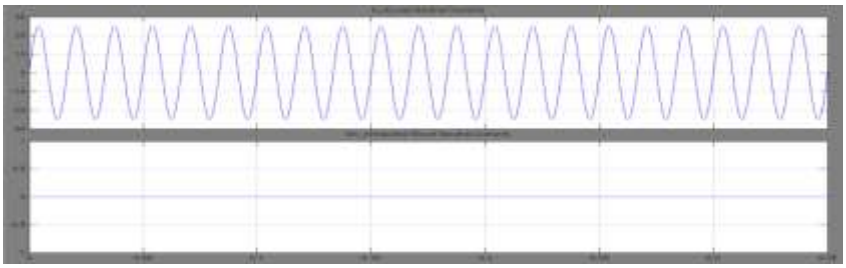

Fig. 22 Load Neutral Current And Injected Shunt Neutral Current

Figure22 shows the load neutral current and injected shunt neutral current.

V.CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. UPQC topology has been proposed in this paper which has the capability to compensate voltage sags, voltage swells and current harmonics at the load at a lower DC-link voltage by using different control strategies for series and shunt APF's. The proposed method is validated through MATLAB simulation

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