

# STUDY THE PERFORMANCE AND DESIGN OF 8051 MICROCONTROLLER USING TANNER TOOLS (V12.5) AND XILINX (6.1I)

**VIJAY KUMAR RAM**

*Dept Of ECE, SCRJET,CCSU, Meerut(UP.), (India).*

## ABSTRACT

*In this paper The innovative power gating are analyzed which minimizes the power dissipation in submicron circuits. The overall view this paper is to attain high speed, low power with alternative logic cells that lead to have reduced power dissipation. Here the total components is designed sub micro technology and observed that power analysis.we investigate the performance of 8051 Microcontroller and the design using Tanner Tools(v12.5),Xilinx(6.1i),Modelsim (SE-5.4a) and Project Navigator also. We start from SPICE code and VHDL code for 16 bit microcontroller simulated the model . We have designed the Schematic and Layout of 8051 microcontroller, using tanner Tools(v12.5) and 0.5 sub micron Technology. We have also done the transient Analysis and DC analysis of above mentioned components using Tanner Tools(v12.5).*

**Keywords:** *8051 Microcontroller, ), Modelsim(SE-.4a), Tanner Tools(V12.5),6Trasister Based RAM ). Xilinx(6.1i).*

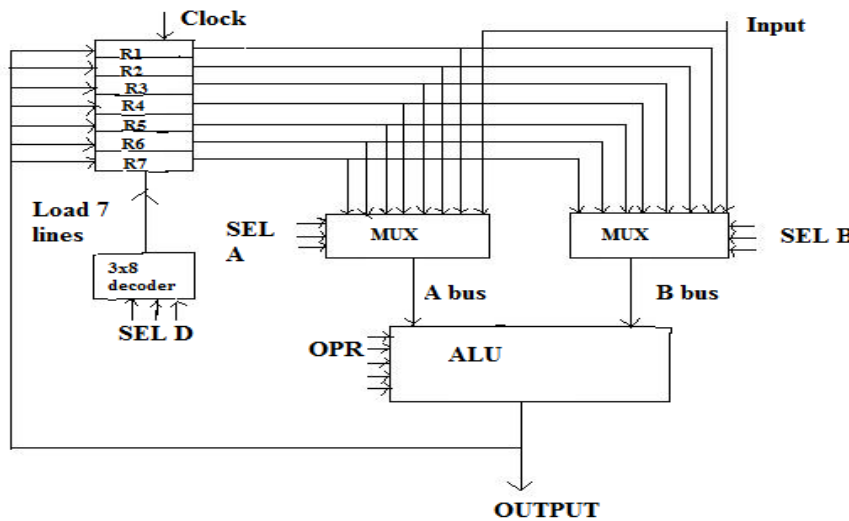
## I INTRODUCTION

As we know that the 8051 microcontroller is the most popular general purpose microcontroller in use today. In this paper we have Analysis of 8051 microcontroller using CPU, RAM and interrupt controller before 8051 microcontroller design onVHDL Language in which check only waveform but we design on Tanner tools(v12.5) and VHDL both and analysis of DC and AC of 8051 microcontroller . We have drawn the schematic of all these three components using Tanner Tools from the schematic we studies the Transient and DC analysis of the above mentioned components. Beside that we have also drawn tools and 0.5 sub micron technology.

## II CPU FOR 8051 MICROCONTROLLER

The Central Processing Unit (CPU) is the brain of the 8051 microcontroller that performs bulk of data- processing operations. In modern computational clusters these issues are usually prevented with the help of jobs and job

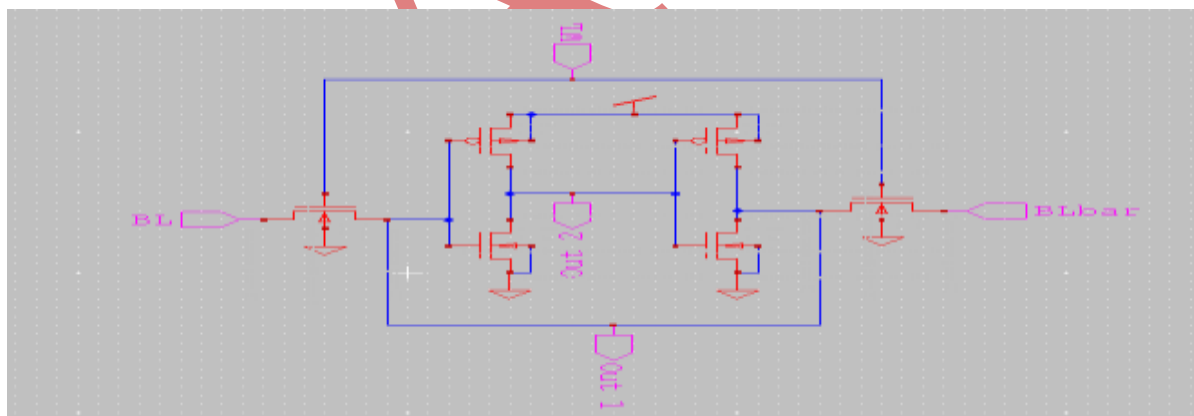
schedulers, which postpone a job and schedule it later, when resources available [2].Figure (1) shown the CPU architecture that we used for (1) drawing its schematic and layout using tanner tools.



**Figure1: Architecture of CPU**

### III 6TRANSISTORS BASED RAM

In this paper we have considered 6 Transistor based RAM. In this RAM out of Six Transistors are used as two inverters and the remaining two transistors are controlled by Word Line Figure (2) shows the circuit diagram of 6T Based RAM . A 128 byte internal asynchronous RAM and other synchronous peripherals including interrupts [3]. Using this, we have drawn schematic of using tanner tools.



**Figure.2 Circuit Diagram of RAM**

### IV INTERRUPT CONTROLLER

Interrupt Controller is a component used to increase the speed of CPU. The Microcontroller includes the SPARC Processor a FPU, a memory controller,an Interrupt Controller and Peripheral devices In a single-chip[4].Figure (3) Shown the circuit diagram of Interrupt Controller Using D Flip Flop. We have used this circuit diagram to Design



**Figure 3 Circuit diagram Interrupt Controller**

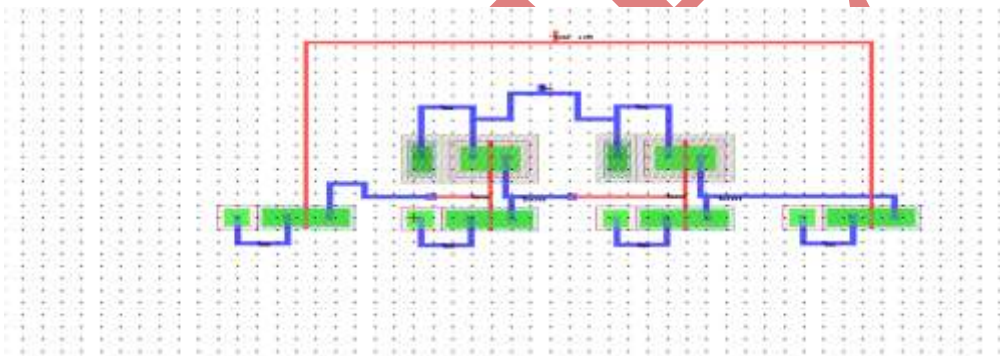
Schematic of Interrupt Controller using Tanner Tool.

## V SIMULATION RESULTS

### 5.1 Schematic Diagram and Layout of RAM

Using Tanner Tools we have designed the schematic and Layout of RAM. Figure (4) shows the schematic diagram of RAM after doing simulation on Tanner Tools. Figure (5) shows the layout of RAM.

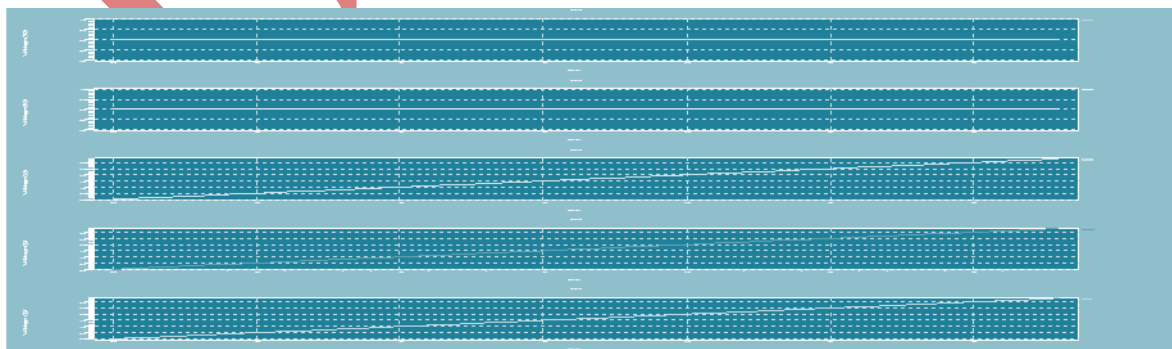
**Figure. 4 Schematic Diagram Of RAM**



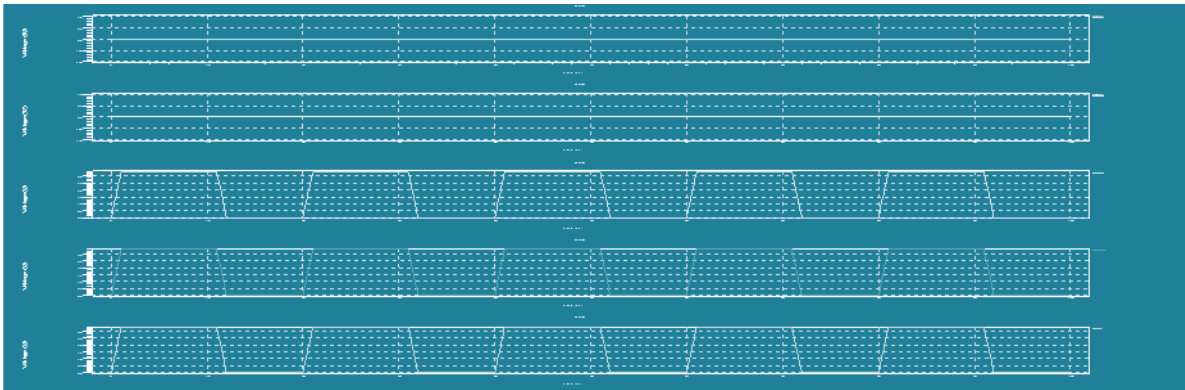
**Figure.5 Layout of RAM**

#### 5.1.1 Transient & DC analysis of RAM

We have done the Transient and DC analysis of RAM using tanner tools. Figure (6) Shown the DC analysis of RAM.



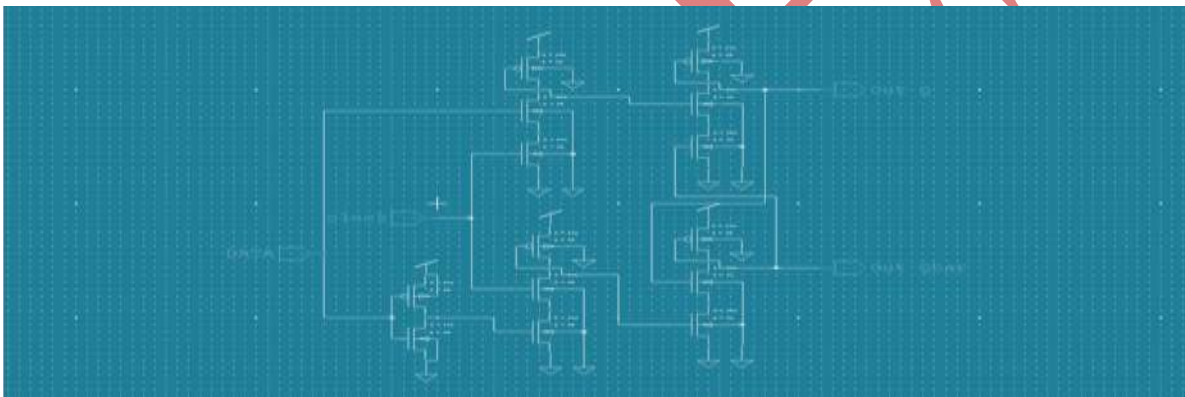
**Figure.6 DC Analysis of RAM**



**Figure.7 Transient Analysis of RAM**

## 5.2 Schematic Diagram of Interrupt Controller

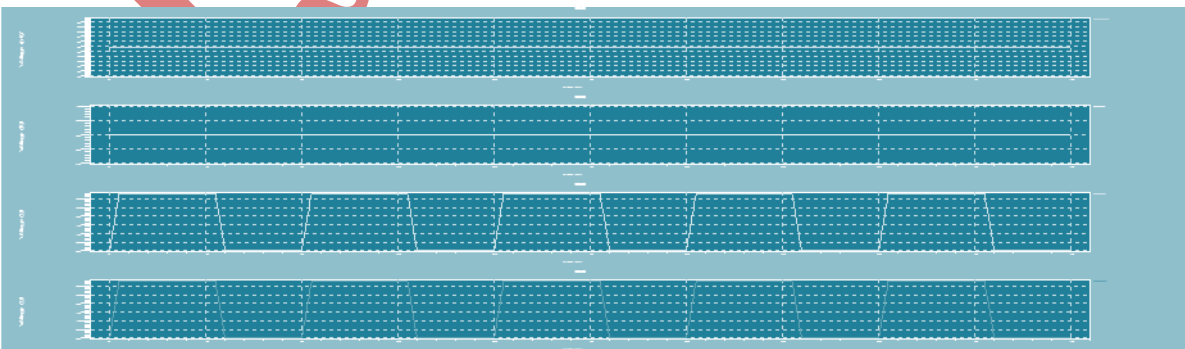
Figure (8) shows the schematic diagram of Interrupt Controller Designed using Tanner Tools.



**Figure.8 Schematic Diagram of Interrupt Controller**

### 5.2.1 Transient & Dc Analysis of Interrupt Controller

Figure.9 & Figure.10 shows the simulation results of Transient and DC analysis of Interrupt Controller using Tanner Tools.



**Figure.9 Transient Analysis of Interrupt Controller**

### 5.3 Schematic Diagram of CPU With Interrupt Controller And RAM

The control unit is used to lessen the Interrupt burden of the main CPU and to reduce the required CPU performance, while message buffer RAM is used to store all messages transmitted and received[7].

Figure(10) shows the schematic diagram of CPU with Interrupt Controller And RAM. We have used Tanner Tools for designing this schematic diagram.

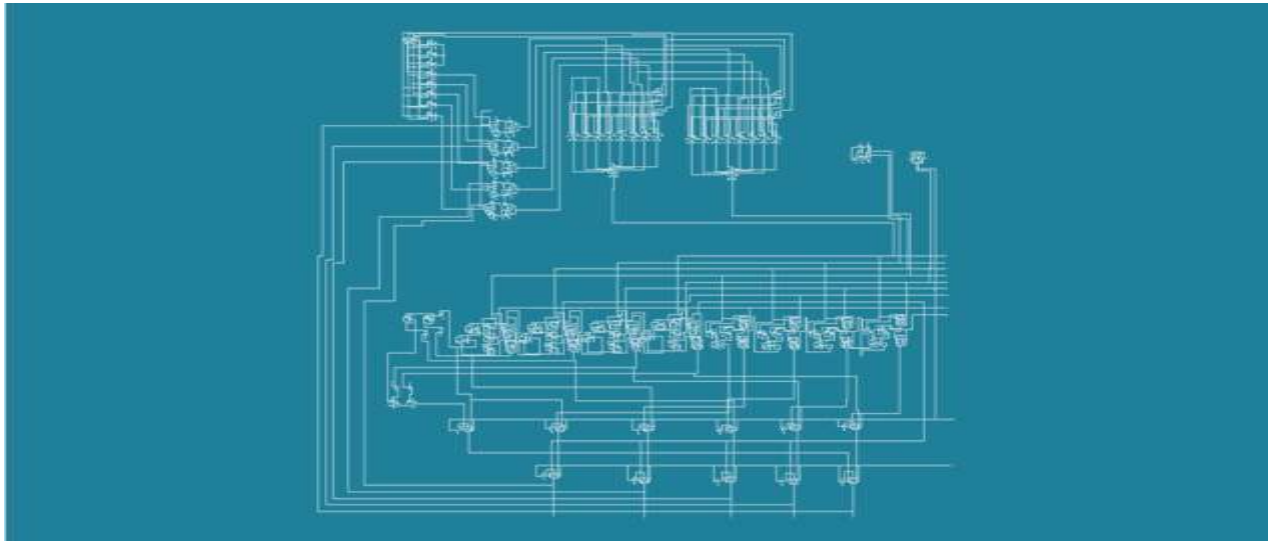


Figure .10 Schematic Diagram of CPU with Interrupt Controller and RAM

#### 5.3.1 Ac & Dc Analysis of CPU with Interrupt Controller And RAM

Transient and DC analysis of CPU with Interrupt Controller and RAM is Shown in Figure (12) & Figure (13).

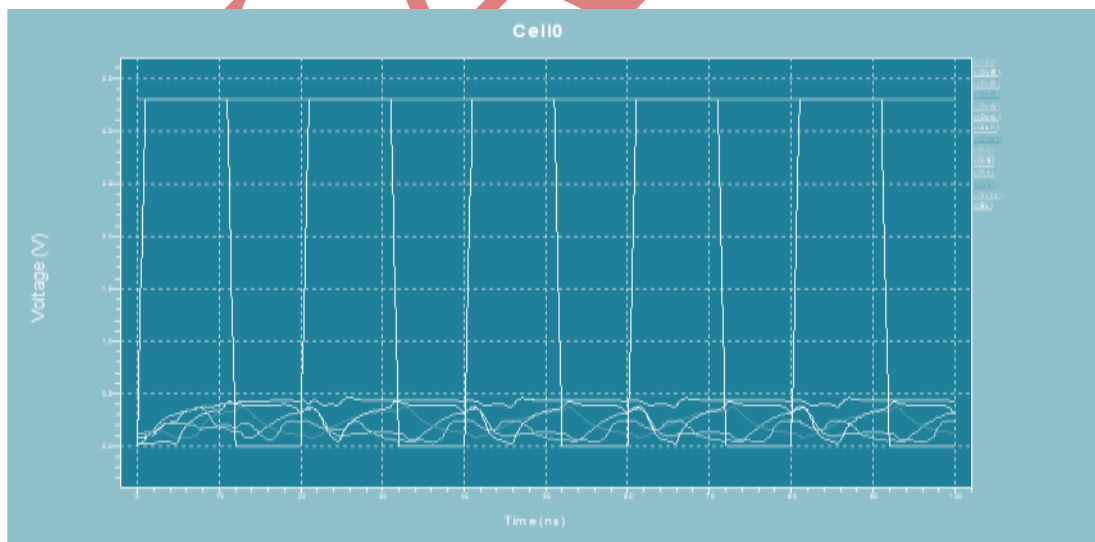
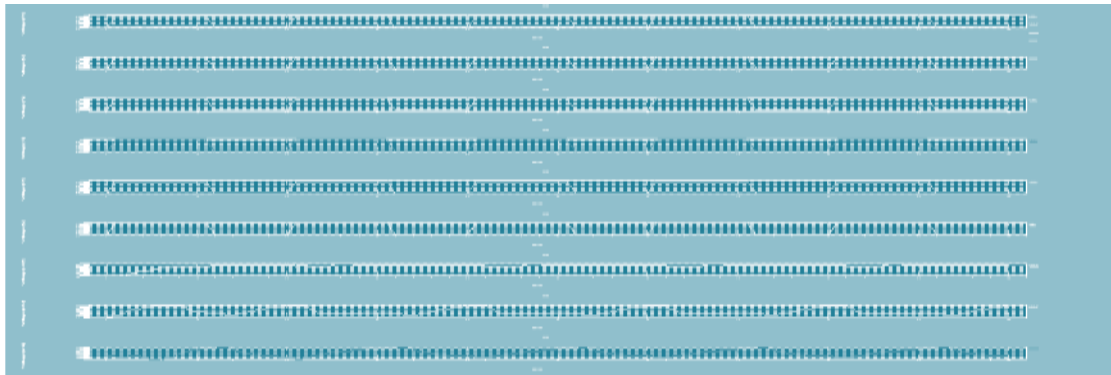


Figure.11 Transient Analysis of CPU with Interrupt Controller and RAM



**Figure.12 DC Analysis of CPU with Interrupt Controller and RAM**

### 5.4 Timing Report of ALU

In CPU architecture, ALU of purely combinational ckt, Independent multiplier and divider module, multi-clocks architecture and hardwired control unit are adopted to get high speed[6].

We have generated the timing report of ALU after doing synthesis on Modelsim (SE-5.4a).

- a) Clock Information: No clock signal found in this design.
- b) Timing Summary: Speed grade=6
- c) Minimum Period: No path found.
- d) Minimum input arrival time before clock: No path found.
- e) Maximum combinational path delay: 61.455 ns.

#### 5.4.2 Waveform of ALU

The performance of the out-of-order architecture will not improve in spite of an expected advance in future technologies[5]. Figure 13 shows the waveform of ALU using Modelsim.



**Figure13 Waveform of ALU**



### 5.5 Timing Report of RAM

The timing report of RAM is generated after doing synthesis on Modelsim.

#### GENERATED AFTER PLACE -AND-ROUTE

##### Clock Information:

Clock Signal	Clock buffer (FF name)	Load
Clock	BUFGP	1201

##### Timing summary:

Speed grade: 6

Minimum period: 13.859 ns (Maximum Frequency: 72.155MHz).

Minimum input arrival time before clock: 31.365 ns.

Maximum output required time after clock: 6.788 ns.

Maximum combinational path delay: No path found.

#### 5.5.2 Waveform of 6T Based Ram

Figure (14) shows the waveform of 6T based RAM using modelsim (SE-5.4a).

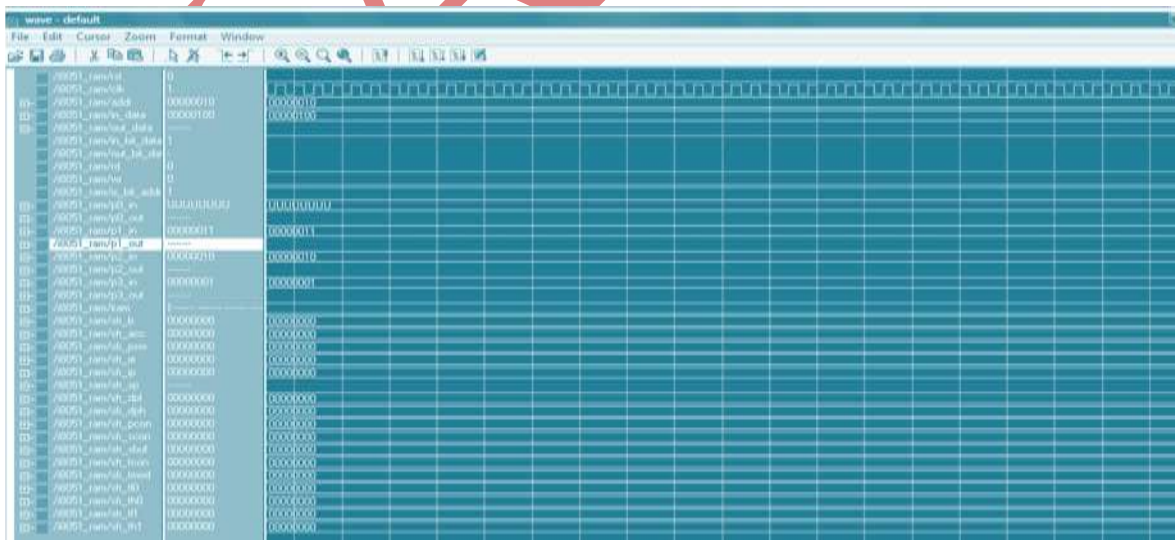


Figure.14 Waveform 6T based RAM

## VI CONCLUSION

We have designed the schematic and layout 8051 microcontroller using tanner tools and studied the transient and DC analysis of 6T based RAM. Interrupt controller of CPU of 8051 microcontroller from timing diagram generated using modelsim (SE-5.4a) .We have shown that when we give on input to Interrupt Controller the speed of CPU increases 30%. If no input is given to Interrupt Controller then there is no change in speed of CPU.

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